Miniature JPL Universal Instrument Bus (UNIIBUS)

Completed Technology Project (2013 - 2017)

Project Introduction

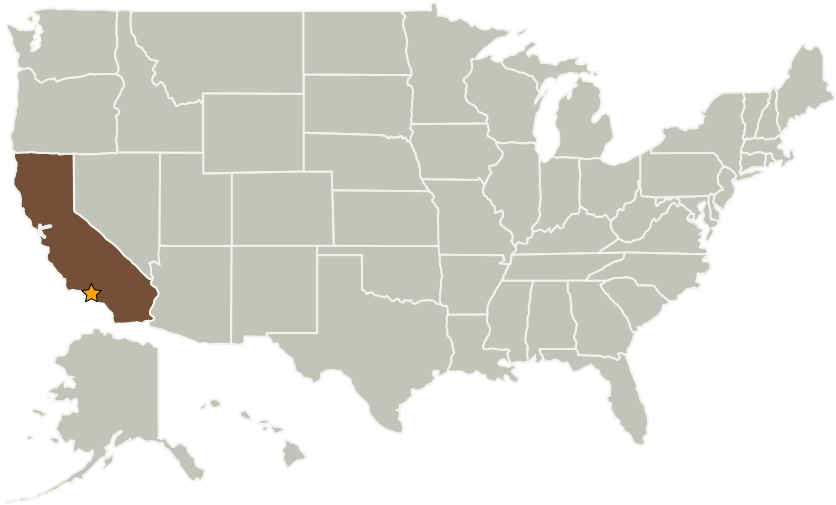
Develop a Universal Digital Processor Bus architecture using state of the art commercial packaging technologies.

This work will transition commercial advanced- yet mature- packaging approaches, such as surface mount and system-in-package, into mainstream use at JPL. Starting with an existing Digital Processor Unit (DPU) board that is planned to be used on multiple spacecraft in the next decade, we will apply modern commercial electronics packaging solutions to create a miniature version of the DPU. The DPU has multi I/O communication options (Spacewire, LVDS, 1553, TTE) and will target a 1U board form factor, down from existing 6U layout. Use performance COTS based devices to provide power and size reduction while maintaining performance and universal adaptability.
The DPU hardware will be used to demonstrate in-house manufacturability, cost effectiveness, functionality, performance, and reliability of state of the art electronics manufacturing and assembly for future-focused NASA missions.
The implementation of newer packaging technologies will result in large decreases in mass, volume, and power of electronic subsystems.

Anticipated Benefits

Can shrink digital command board size by >40%. Improved signal and power efficiency has a positive effect on the entire flight system through reductions in IO count, cost, mass and volume. Improvement in manufacturing costs and increased reliability. Ready availability of components with shorter lead time and lower cost.

Primary U.S. Work Locations and Key Partners



Miniature JPL Universal Instrument Bus

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Organizational Responsibility

Responsible Mission Directorate:

Mission Support Directorate (MSD)

Lead Center / Facility:

Jet Propulsion Laboratory (JPL)

Responsible Program:

Center Independent Research & Development: JPL IRAD

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Organizations Performing Work	Role	Type	Location
★Jet Propulsion Laboratory(JPL)	Lead Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations
California

Project Management

Program Manager:

Fred Y Hadaegh

Project Manager:

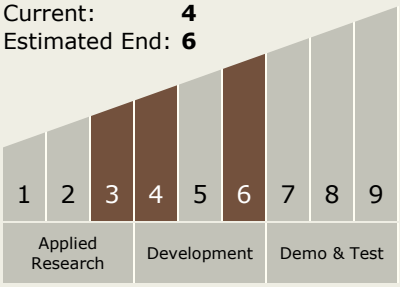
Jonas Zmuidzinas

Principal Investigator:

Don J Hunter

Technology Maturity (TRL)

Start: **3**
Current: **4**
Estimated End: **6**



Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.2 Electronic Packaging and Implementations